ISSN: 0975-8585

Research Journal of Pharmaceutical, Biological and Chemical Sciences

Investigation on Adders and Multipliers For ALU.

R Rashvenee[1], Roshini Keerthana D[2], T Ravi[3]*.

[1,2]BE Electronics and Communication Engineering, Sathyabama University, Chennai, Tamil Nadu, India.
[3]Assistant Professor, Department of ECE, Sathyabama University, Chennai, Tamil Nadu, India.

ABSTRACT

ALU is the most important unit of a processor. The computing efficiency of the processor depends totally on the efficiency of the ALU. The adder is the basic block of the ALU which does all the arithmetic and logic operations. The main factors are delay, power and area which decide the efficiency of the ALU. Multiplier is the major efficiency factor in ALU. Parallel prefix adders have better delay performance; it involves the execution of the operation in parallel. In this paper all the PPAs are surveyed on and the best PPA is fitted in the most efficient multiplier in order to make the ALU more efficient in terms of speed, area and power.

Keywords: PPA, Vedic Multiplier, Delay, Power, Area

Corresponding author

ISSN: 0975-8585

INTRODUCTION

VLSI is the process of integrating thousands of transistors into a single chip. VLSI design is mainly used to minimize the interconnecting fabrics area. The main factors which limit the development of smaller and more complex IC chip are the IC fabrication technology, designer productivity and the cost. Depending on the application, different performance aspects become important. An ALU is an integral part of a processor. It performs all the arithmetic and logical operations. Fast and accurate operation depends on the performance of multiplier. Hence improving the performance of the multiplier improves the efficiency of the ALU. In order to increase the performance of a multiplier we need to make the adder more efficient. Binary addition is the most fundamental and important arithmetic function where the adder should be fast and efficient in terms of area, power and speed. Its seen that than conventional adders such as ripple carry adder, carry look ahead adder, carry select adder, etc., the parallel prefix adders are more efficient. These adders can be used in a multiplier. The Booth, Wallace, Array multipliers have all been implemented in an ALU, but the multiplier implemented by using the Vedic sutras have been showing high performance when implied in an ALU. Section 1 of this paper shows the introduction, followed by Section 2 which describes about the Parallel Prefix adders and Section 3 which explains about the multipliers. The paper has been concluded in Section 4.

PARALLEL PREFIX ADDERS

The binary adders are having the propagation delay and carry chain problems. To reduce the carry propagation delay, most of the adders have been represented as parallel prefix adder structure consisting of pre-processing, carry look ahead and post processing sections. The parallel prefix adders' delay is directly proportional to the number of levels in the carry propagation stage. Below is the performance survey of six different parallel prefix adders.

A. KOGGE STONE ADDER

The Kogge Stone Adder is a parallel prefix form of carry look ahead adder. It's widely considered as the fastest adder design possible. The structure of 8 bit Kogge Stone Adder is given in Figure 1. This adder is widely used for applications which require high performance. The concept of Kogge Stone adder is almost the same as that of the carry look ahead adder except for the following steps (L=2), called parallel carry prefix chain. At first when (L=1), it generates and propagates of 2-bit are computed at the same time. In the second level where (L=2), it generates and propagates of 4-bit which is calculated by using the result of 2-bit in level 1. Therefore, when the calculations of level 2 are being computed, the actual carry value of the 4th bit would be available. In the third level (L=3), the carry-out value of the 8th bit is computed by using the carry result of the 4th bit. The same method is adopted in level 3 and is applied to get the carry-out values of the 16th bit and the 32nd bit in level 4 and level 5 and so on. All other carries of each bit are also computed in parallel. This Kogge stone adder has the least delay but doubles up in area [2][3] and has high power consumption than all other adders [5].

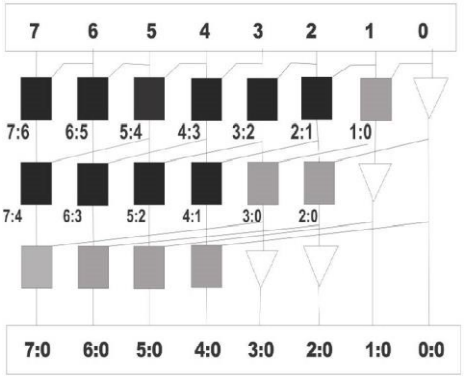

Fig1. 8 bit Kogge Stone Adder

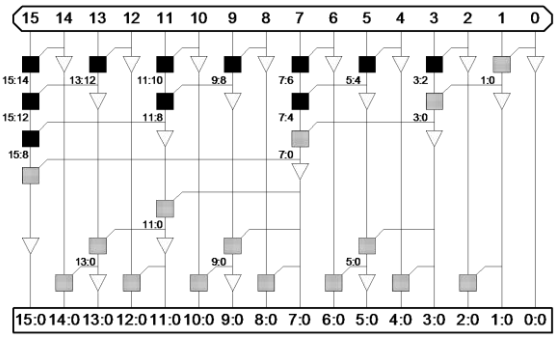

Fig 1. Brent kung Adder

ISSN: 0975-8585

B. BRENT KUNG ADDER

Brent Kung is a parallel prefix form of the carry look ahead adder. The block diagram of 16 bit Brent Kung adder is shown in Figure 2. In carry look ahead adder, as the size of the input operands increase the delay is also increased. The idea in [2] is to have a gate level depth of O(log2(n)). It takes lesser area to be implemented when compared to other prefix adders such as Kogge Stone adder and it also has less wiring. The method shown in [2] is being used to calculate the output of a carry chain. This will reduce the delay without compromising the power performance of the adder. But the method used in [2] has not reduced delay to a great extent. The area consumption and power is the lowest in BKA than any other adder [2, 5].

C. KNOWLES ADDER

Knowles adder is similar to Kogge Stone Adder, but it has different logic to calculate the output. The below figure 3 illustrates the method used in [2]16-bit Knowles Adder. Knowles adder has high area but lesser than that of Kogge Stone Adder [2]. The delay of this adder is as same as that of Kogge stone adder which makes it more efficient than that of KSA [2,6].

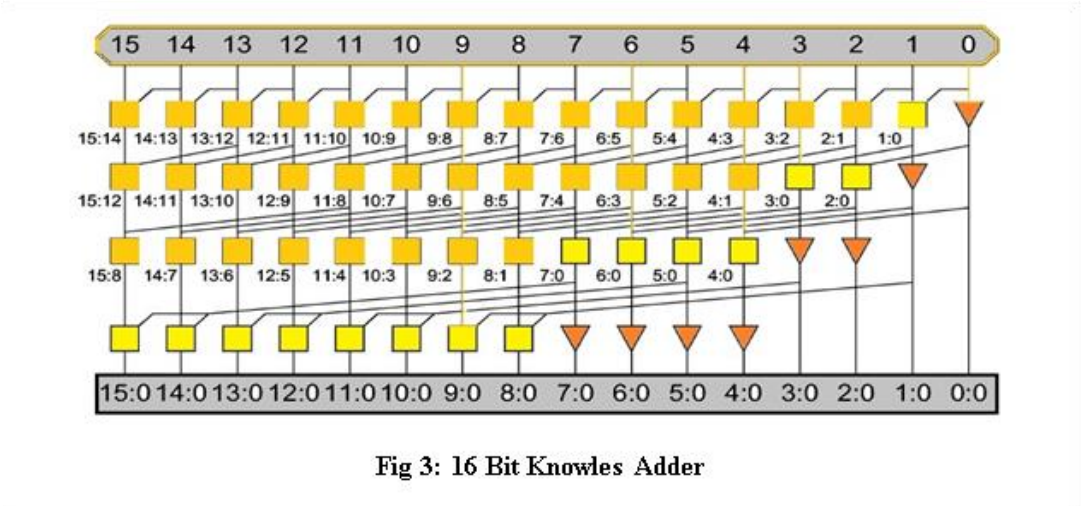

Fig 3: 16 Bit Knowles Adder

Sudheer Kumar Yezerla et al., 2014 [8] worked on the delay, power and area for parallel prefix adders which shows that 16 bit STA used terminates with the ripple carry adder and uses black cells, gray cells and full adders but the interconnection between them is different. The 16 Bit Brent Kung adder used 14 black cells and 11 gray cells which is comparatively lesser to KSA and occupies less space than KSA. There was 5.77% increase of delay for RCA and for KSA it was improved by 19.28%.

Sunil M et al., 2015 [9] worked on implementing a faster Kogge stone adder. The Kogge stone adder is faster but the area of consumption is high, therefore here the black cells were reduced and the wires were rerouted to achieve lesser area and also higher speed. The modified Kogge stone showed better performance than normal KSA. The logic delay and routing delay of MKSA was 4.998ns which was 9.84% lower than normal KSA.

M. Prasanna Kumar et al., 2015 [4] researched on the comparison of Brent Kung adder and Kogge Stone adder. It has been written in VHSIC Hardware Description Language source file. The results were in the form of RTL diagram and functional waveform. The synthesis report was obtained in the form of gate count for the area, delay and power consumption. It shows that BKA area rises as the bit size increases but not as drastically as KSA. In terms of delay also BKA shows good performance but not better than KSA.

MeghaTalsania et al., 2009 [5] worked on different parallel prefix adder to find out the optimal adder modules that can be used for the realization of high speed and low power adder structures. The addition algorithms of six different parallel prefix adders were studied. The performance analysis was based on the silicon area required for the implementation of the algorithm in hardware, the power dissipation during computation, and the worst case delay in performing the operation. In this the KSA showed best performance

in terms of delay and BKA showed the best performance in terms of power consumption and area. Even Knowles Adder showed the best delay performance for 16-bit width.

Deepak Raj et al., 2015 [2] researched on comparison of serial adders with parallel prefix adders. The results show that parallel prefix adders are better in term of delay and at the same time there is a trade off with the area occupied. The paper mainly shows that KSA is the faster compared to BKA and other serial adders. The area is lowest for BKA. The results are shown below in Table 1, which shows that the delay is least in Kogge stone adder but the area is higher by twice than BKA.

Table 1. Adders Synthesis report [2]

Design Utilization Summary (SPARTAN 3)				
Adder	No. of Slices	No. of 4 input LUT's	No. of bounded IOB's	Delay (ns)
RCA	18	31	49	27.34
CSA	21	37	50	33.98
CLA	18	32	50	28.741
KSA	41	72	50	18.588
BKA	21	38	50	23.854

MULTIPLIERS

ALU is the heart of any complex systems.ALU is required to increase the speed of any system. To increase the speed and to reduce the delay of the ALU multiplier is used. Multiplier is the very important functioning part of the ALU in case of increasing the speed. All the multipliers are surveyed and here we are using the Vedic Multiplier to reduce the delay and to increase the speed of the speed of the system. When compared all the other Multiplier Vedic Multiplier is more efficient.

A. ARRAY MULTIPLIER

Array multiplier is familiar due to its structure and its circuit is based on add and shift algorithm. Every partial product is obtained by the multiplication of the multiplicand with one multiplier bit. The partial product is shifted according to their bit orders and then added [6,7]. In order to construct a small multiplier, the partial product values are added iteratively. The partial product is kept in a register and it is initialized to 0. On every cycle, if the low-order bit of the multiplier is 1 the multiplicand is added to the partial product, then the multiplier is shifted one bit to the right where the multiplicand is shifted one bit to the left. This method uses only a single adder; hence it is much smaller than the full adder array.

B. BOOTH MULTIPLIER

To treat both positive and negative numbers uniformly powerful algorithm for signed-number multiplication is employed. For the standard add-shift operation, each multiplier bit generates one multiple of the multiplicand that is added to the partial product. If the multiplier is very large, a large number of multiplicands have to be added. This leads to the delay of multiplier and is determined mainly by the number of additions performed. The performance will get better if the number of the additions is reduced in some way [6]. Booth algorithm is a method that will reduce the number of multiplicand multiples. But for a given range of numbers to be represented, a higher representation is needed.

C. WALLACE TREE MULTIPLIER

Wallace tree multiplier is one of the fastest multipliers when compared with simple array multiplier and it is a parallel multiplier. To reduce the latency, it uses carry save addition algorithm. The researchers aim at achieving higher speed and lower power consumption even while occupying reduced silicon area. Wallace tree basically multiplies two unsigned integers where the new architecture enhances the speed performance of the widely acknowledged WTM.

ISSN: 0975-8585

D. VEDIC MULTIPLIER

Vedic mathematics is used to solve the complex calculations involve in usual mathematics. Owing to its simple strategy, which mainly includes natural viewpoints of human being, it leads to a straightforward process. It consents to incorporate the arithmetic rules along with high speed and easy implementation, thereby viable for a range of applications based on computing. Vedic mathematics is the ancient system used for doing fast calculations in the mathematics. Vedic mathematics for computation of algorithms of the coprocessor will reduce the computational time, power, area, etc. Vedic mathematics is based on the 16 sutras [3]. This system is more simple and faster than the modern mathematics. The Urdhava Tiryakbhyamsutra based multiplier architecture is shown in figure 4.

Navneetdubey et al. (2014) worked on the design of the multiplier using Booth Algorithm where the proposed ALU can be designed using Verilog HDL.In this the Booth Multiplication Algorithm reduces the hardware complexity and provide output faster than other multipliers.Due to less area and faster operation of the Booth Multiplier makes the ALU to work faster [6].

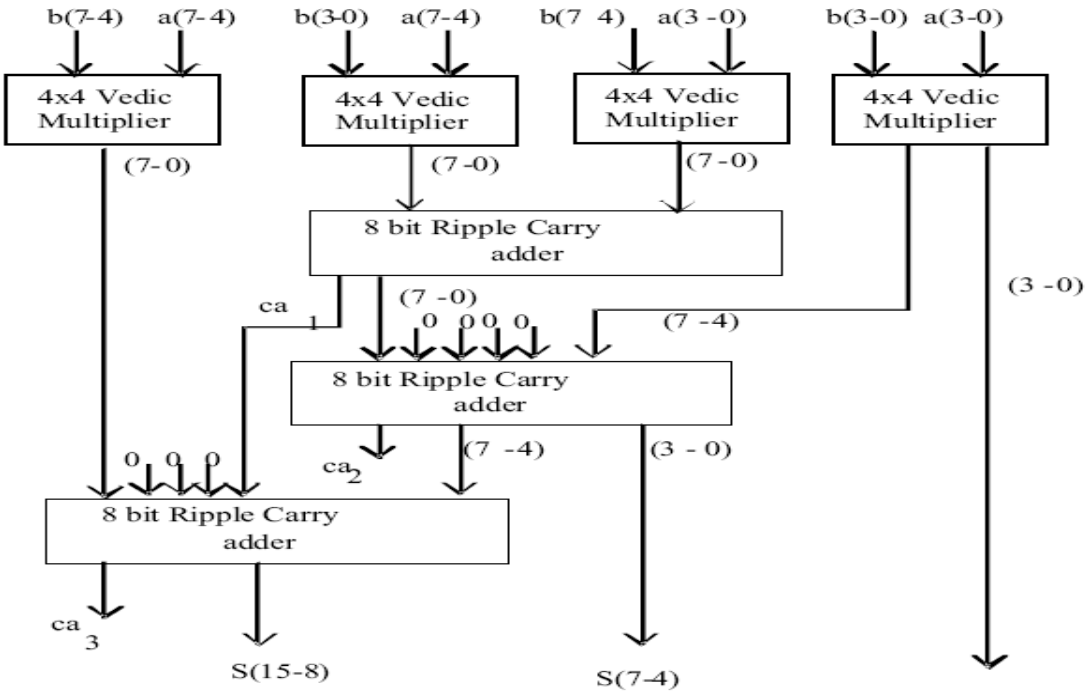

Fig 4:8X8 Vedic Multiplier

V.Vijayalakshmi et al. (2014) did research to reduce the delay and to increase the speed of the ALU using Vedic Multiplier. Here the different types of multipliers are surveyed and according to the final synthesis report it is proved that Vedic Multiplier is more efficient than the other multipliers for reducing delay and to increase the speed [3].

Prof.VipinBhure et al. (2014) designed a low power 64 bit ALU, which is using Verilog and the consumption of low power is achieved with Vedic Multiplier. Here the UrdhvaTriyakbhyamsutra is used from Vedic Mathematics. The most important part of this issue is the speed is increased ad the area is decreased [7].

V.P.Gejji et al. (2015) worked on the high performance ,high throughput an area efficient architecture of the ALU.The most important part of the ALU is that the developed multiplier architecture is based on vertical and crosswise structure of Vedic Mathematics.The Vedic Multiplier have been implemented in Spartan device to reduce the delay.According to the synthesis report the Vedic Multiplier are much more efficient than the conventional multiplier[1].

Table 1: Path Delay Comparison Table for Multipliers [1]

Design	Path delay (ns)	No. of 4 input LUT (out of 1536)	IOB (out of 140)	I/O'S	No. of slices (out of 768)
Array 8bit	89.078	182	32	32	103
Booth 8bit	36.808	237	34	34	120
Vedic 8bit	23.707	133	32	32	77
Array 16bit	81.989	661	64	64	378
Booth 16bit	76.670	993	66	66	499
Vedic 16	42.436	571	64	64	323

CONCLUSION

From the literature on Parallel Prefix Adders used in ALU, it shows that PPA are much faster and efficient than conventional adders (RCA, CSA, LKA). The Kogge stone adder is the most efficient adder when it comes in terms of speed as it's the fastest adder design available, but it's area and power is very high. If an ALU is to be designed to reduce area and power consumption Brent kung adder would be a more efficient than KSA. So as to design an ALU which is more efficient its best to use Brent Kung Adder. From the various multipliers used in ALU, the developed multiplier architecture which is based on vertical and crosswise structure of Vedic Mathematics have been implemented in Spartan device to reduce the delay. According to the synthesis report obtained, it shows that the Vedic Multiplier is much more efficient than the conventional multiplier.

REFERENCES

[1] Akshata.R,Kanchan A.Joshi,Prof.V.P.Gejji,"Analysis And Implementation Of Vedic Multiplier FPGA", International Journal For Technological Research In Engineering, Volume 2, Issue 9, May 2015,PP 2181-2183.

[2] Deepak Raj, Sahana, Prof. Praveen J, Prof.Raghavendra Rao R," Design and Implementation of Different Types of Efficient Parallel Prefix Adders," International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering, Volume 3, Special Issue 1, April 2015

[3] Ravi.T "Design and performance analysis of ultra low power RISC processor using hybrid drowsy logic in CMOS technologies" International Journal of Applied Engineering Research (IJAER) Volume 10, Number 2 (2015) pp. 4287-4296.

[4] M. Prasanna Kumar, V. Siddharthan, Dr. K. Gopalakrishnan," Comparative Analysis of Brent Kung &Kogge Stone Parallel Prefix Adder for their Area, Delay and Power Consumption", Indian Journal of Applied Research, Volume 5, Issue 10, October 2015

[5] MeghaTalsania, Eugene John," Comparative Analysis of Parallel Prefix Adders", A Comparative Analysis of Parallel Prefix Adders 12th Euromicro Conference on Digital System Design, Architectures, Methods and Tools (2009), pp. 281–286

[6] S.Ranjith[1], T.Ravi[2], P.Umarani[3], R.Arunya[4] "Design of CNTFET based sequential circuits using fault tolerant reversible logic" International Journal of Applied Engineering Research Volume 9, Number 24 (2014) pp. 25789-25804

[7] Prof.PranaliThakre, Dr.SanjayDorle, VipinBhure, "Low Power 64 Bit Multiplier By Vedic Mathematics", International Journal Of Application Or Innovation In Engineering And Management, Volume 3, Issue 4, April 2014 ,PP 393-396.

[8] Sudheer Kumar Yezerla, B Rajendra, "Design and Estimation of delay, Power and area for Parallel Prefix Adders," Proceedings of 2014 RAECS UIET Panjab University Chandigarh, 06-08 March, 2014, ISBN: 978-1-4799-2290-1, IEEE

[9] Sunil M, Ankith R D, Manjunatha G D, Premanandha B S," Design and Implementation of Faster Parallel Prefix Kogge Stone Adder", International Journal of Electrical and Electronic Engineering & Telecommunications, ISSN 2319 – 2518, Vol. 3, No. 1, January 2014.